

CSEE 4280: Lab 6:

Designing the Toy Processor Datapath

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Contributions: Please list contributions (in estimated percentages) of each member in the following categories.

• Pre-lab design and analysis:

Habilou - 50% Kingsley - 50%

• In-lab module and testbench design

Habilou - 50% Kingsley - 50%

• In-lab testbench simulation and analysis

Habilou - 50% Kingsley - 50%

• In-lab FPGA synthesis and analysis

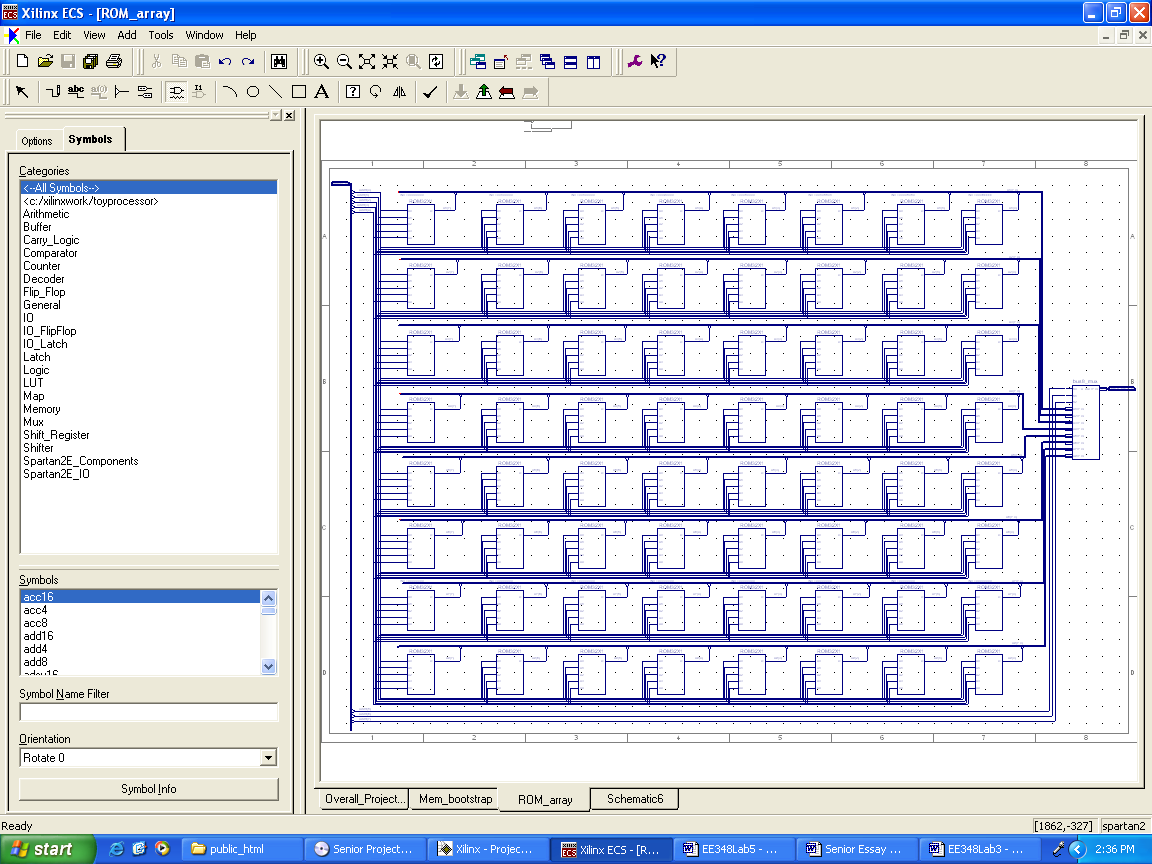
Habilou - 50% Kingsley - 50%

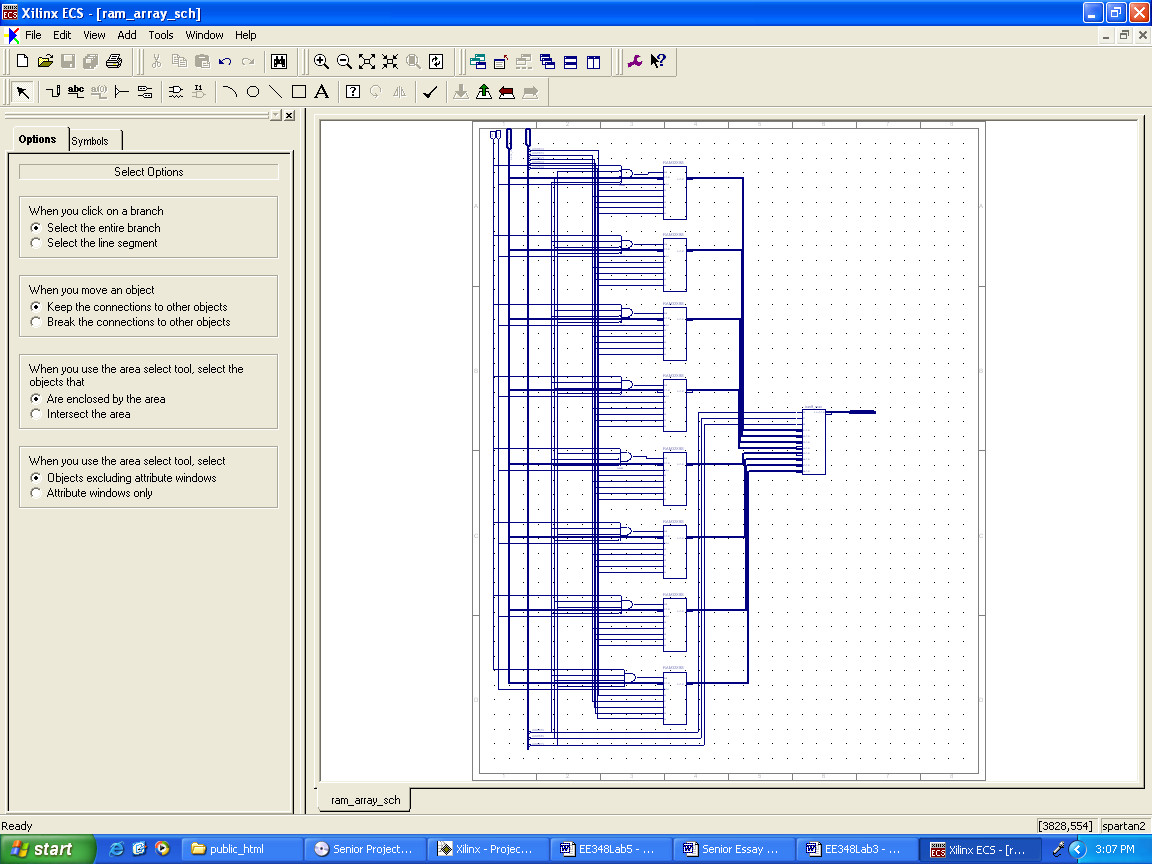
• Lab report writing

Habilou - 50% Kingsley - 50%

# **ABSTRACT**

In the previous labs you built a processor. It can execute instructions defined if we do not have to access the memory — the processor you built so far has no memory. In this lab, we will include a Random-Access Memory (RAM) and a Read Only Memory (ROM) memory for our processor. Once we put everything together, we can load our processor design onto the Xilinx FPGA board. After that, you can write any simple program in machine code, load it into your processor, and execute the program on the Basys2 board.

1. **INTRODUCTION**
   1. **Components to be included**
      1. **ROM\_array**
      2. **RAM\_array**



1. **IMPLEMENTATION DETAILS**
   1. **Prelab**

**My partner and I submitted our prelab before going on break.**

* 1. **Memory Bootstrapping Schematic  
       
     A screen shot of a computer

     Description automatically generated**
  2. **ROM**
     1. **ROM Testbench  
        A screenshot of a cell phone

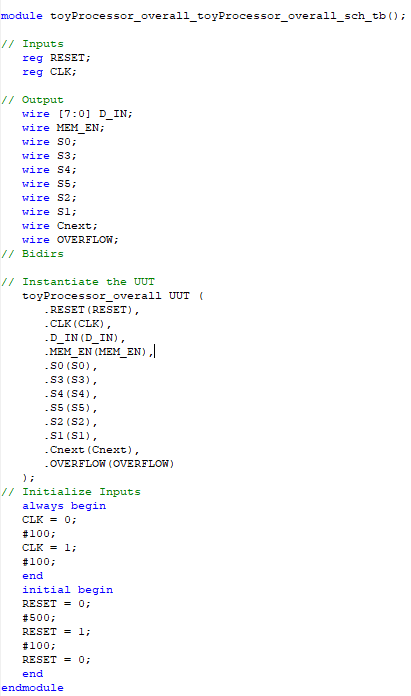
        Description automatically generated**
     2. **A picture containing screenshot, dark, sitting, player

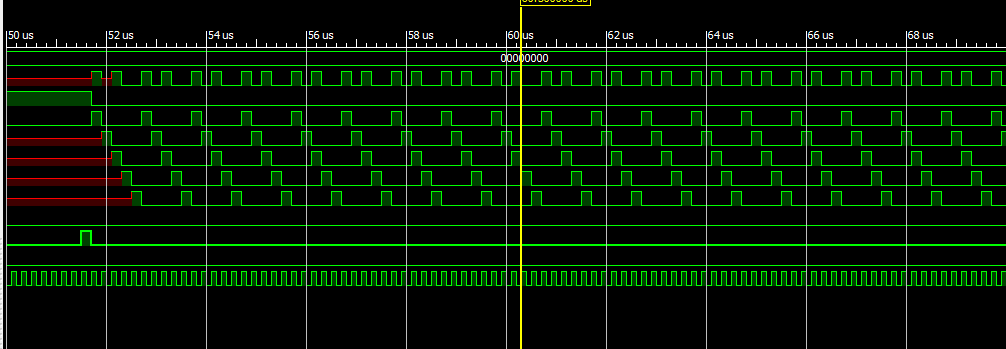
        Description automatically generatedROM Waveform**
  3. **RAM**
     1. **A screenshot of a cell phone

        Description automatically generatedRAM Testbench**

* + 1. **A picture containing indoor, scoreboard, black, sitting

       Description automatically generatedRAM Waveform**
  1. **Overall** 
     1. **A close up of a piece of paper

        Description automatically generatedOverall Schematic**
     2. **Overall Testbench**
     3. **Overall Waveform**

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**The Waveform obtained confirms the correctness of our module because we were able to replicate the waveform given in the lab instruction.**

1. **CONCLUSION**

We were able to create a controller and confirmed its functionality by creating a testbench and obtaining a waveform identical to the one given in the lab instruction.